

Fig. 1
(Prior Art)

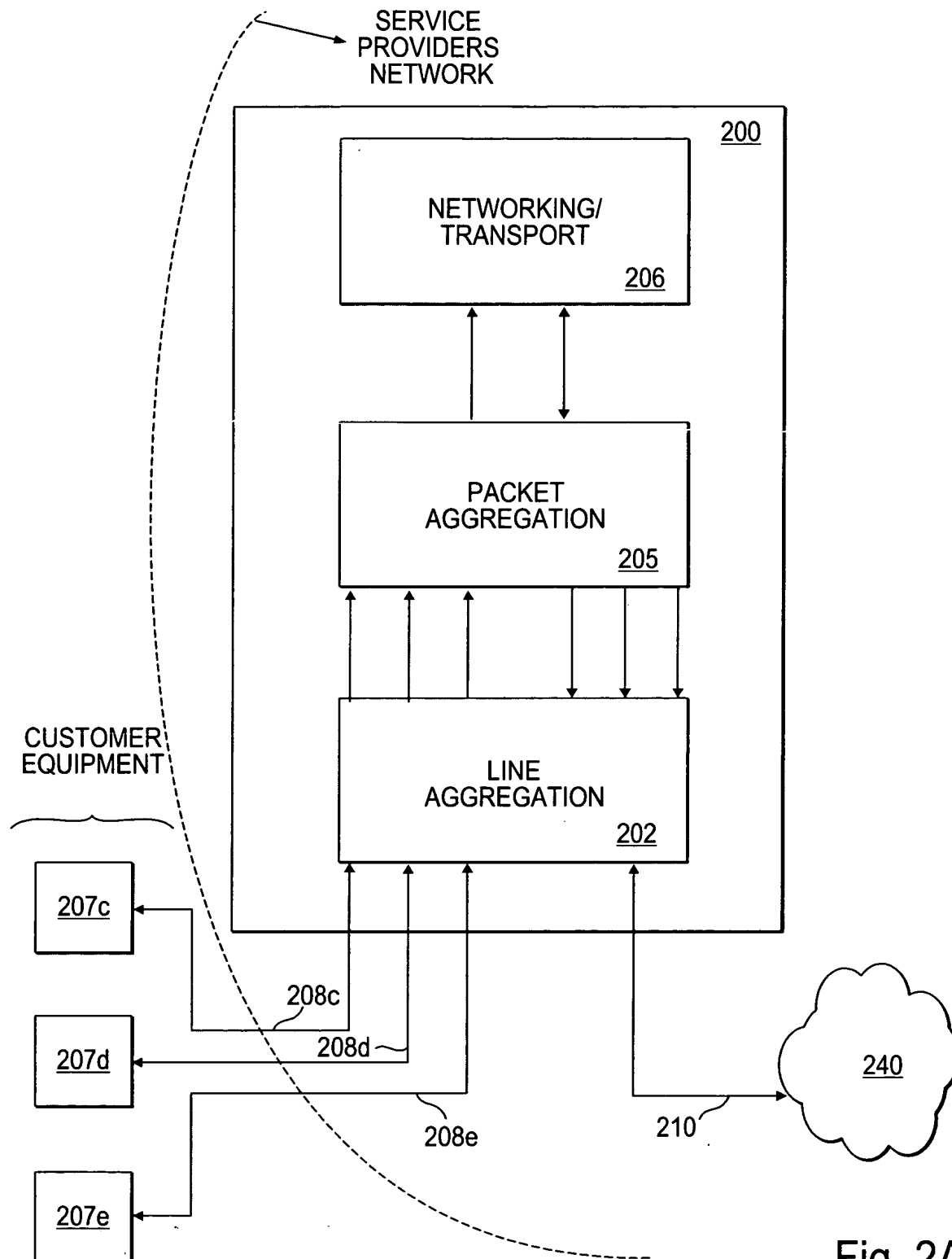


Fig. 2A

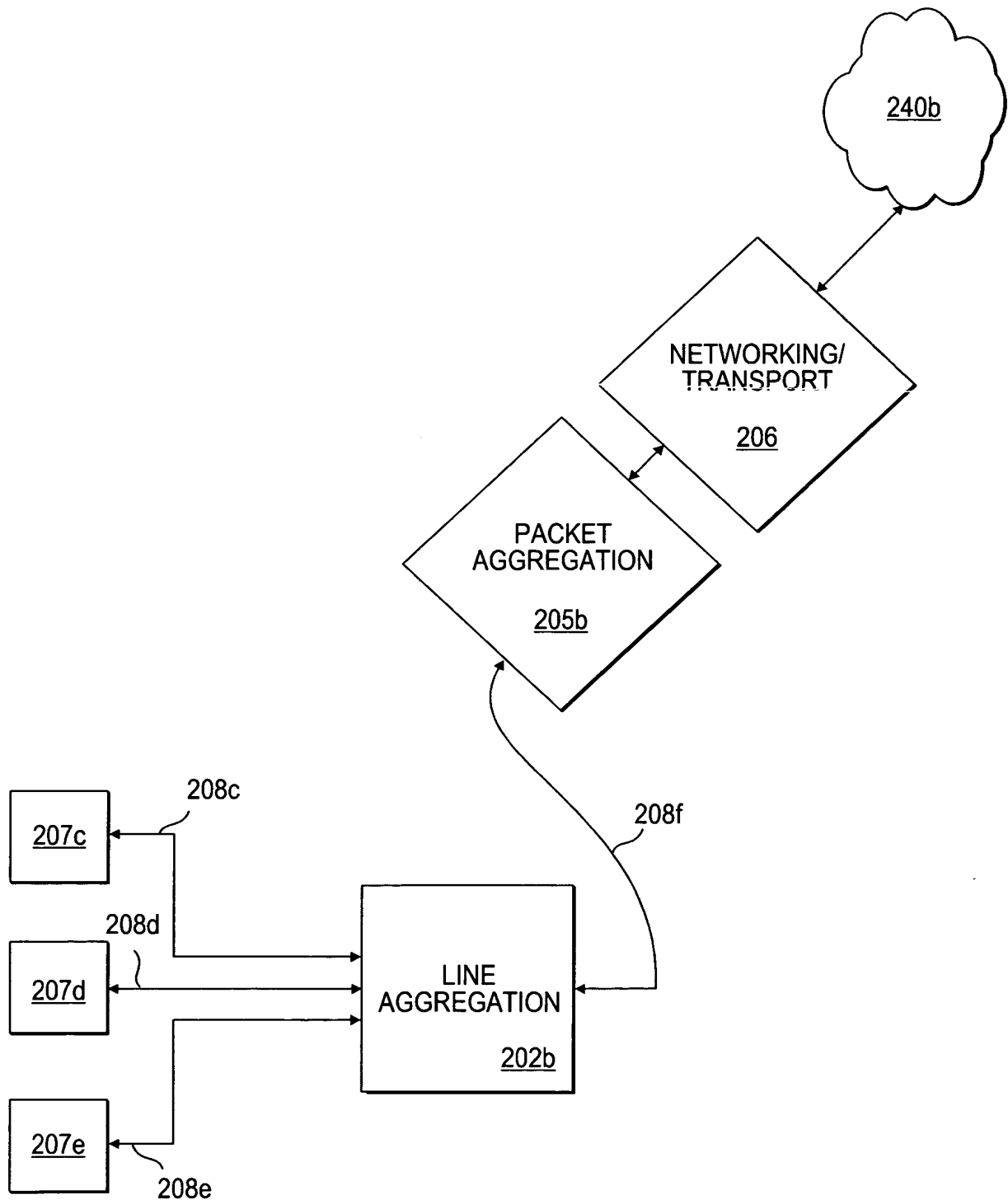


Fig. 2B

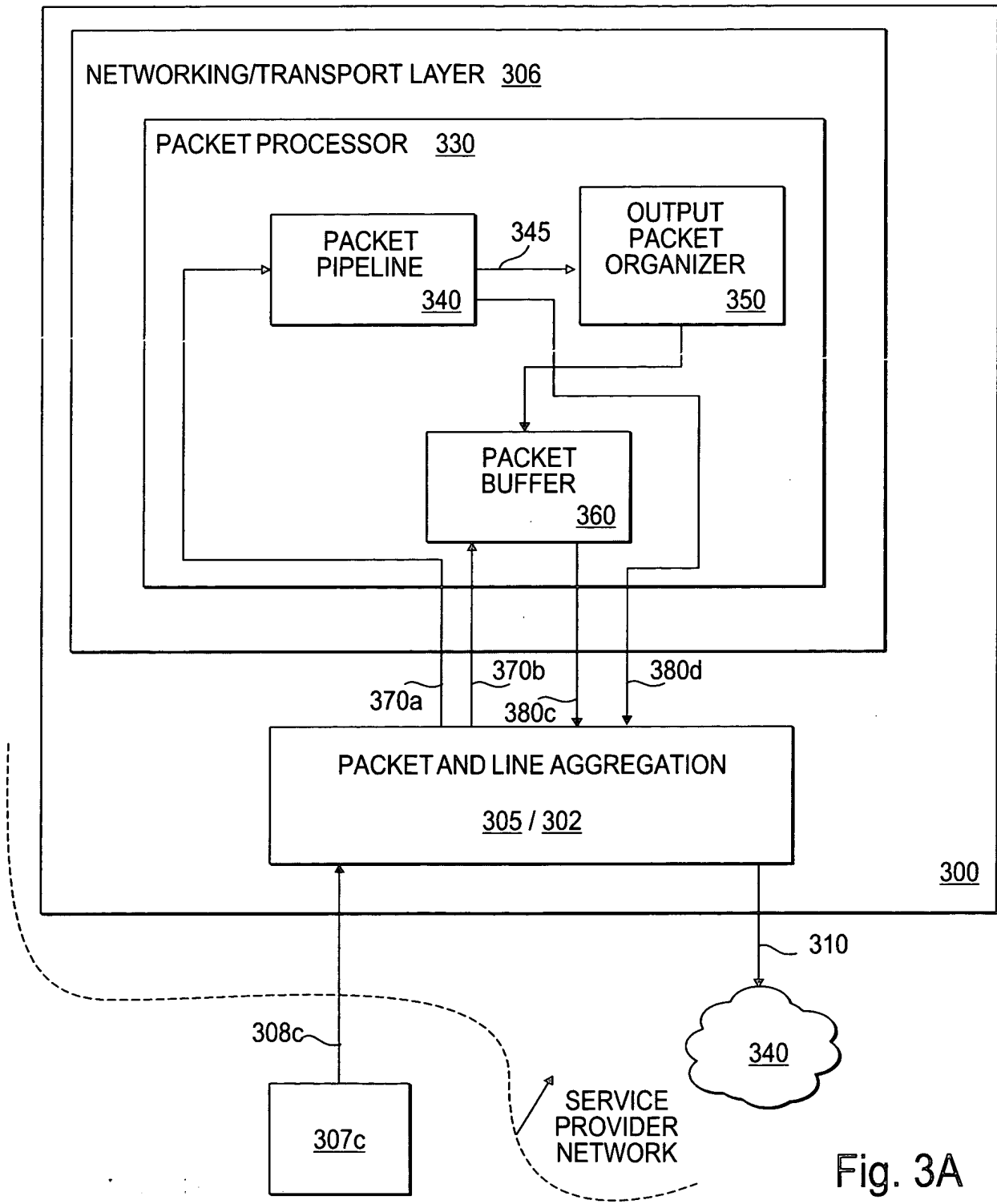


Fig. 3A

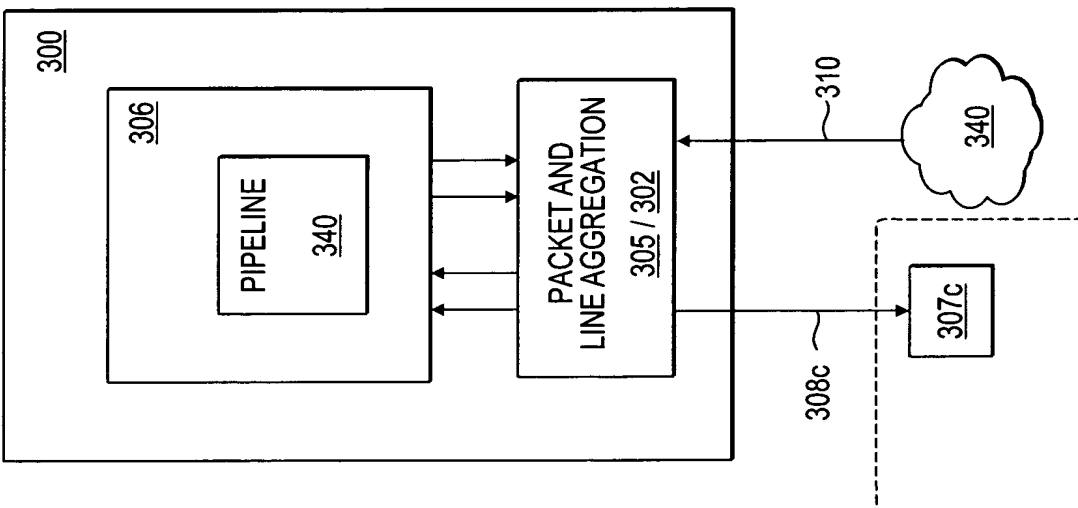


Fig. 3B

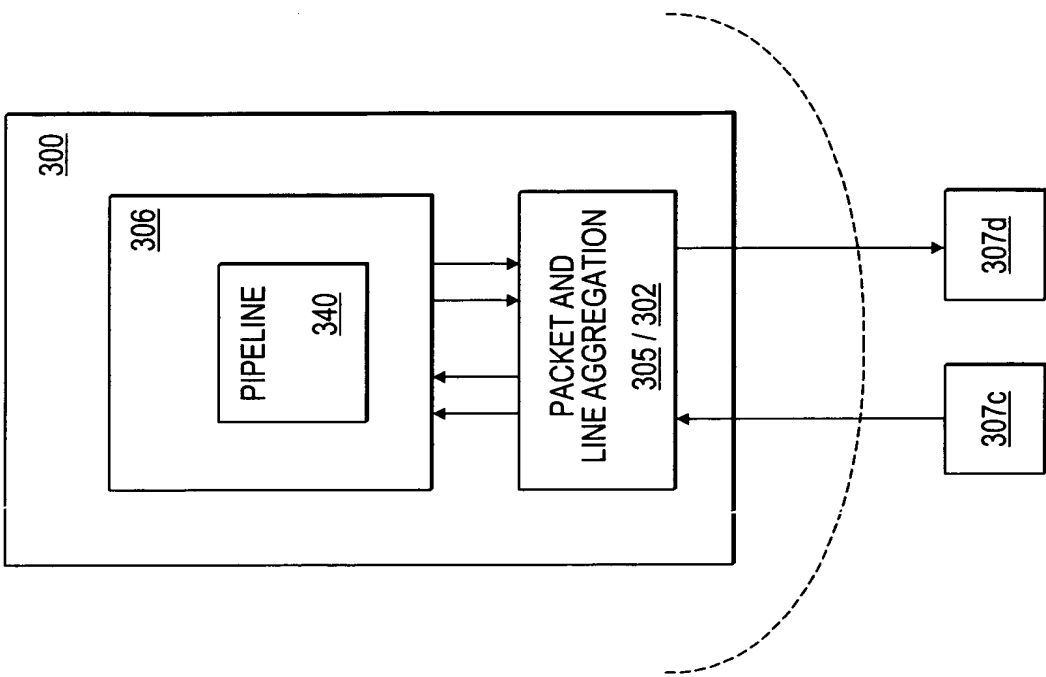


Fig. 3C

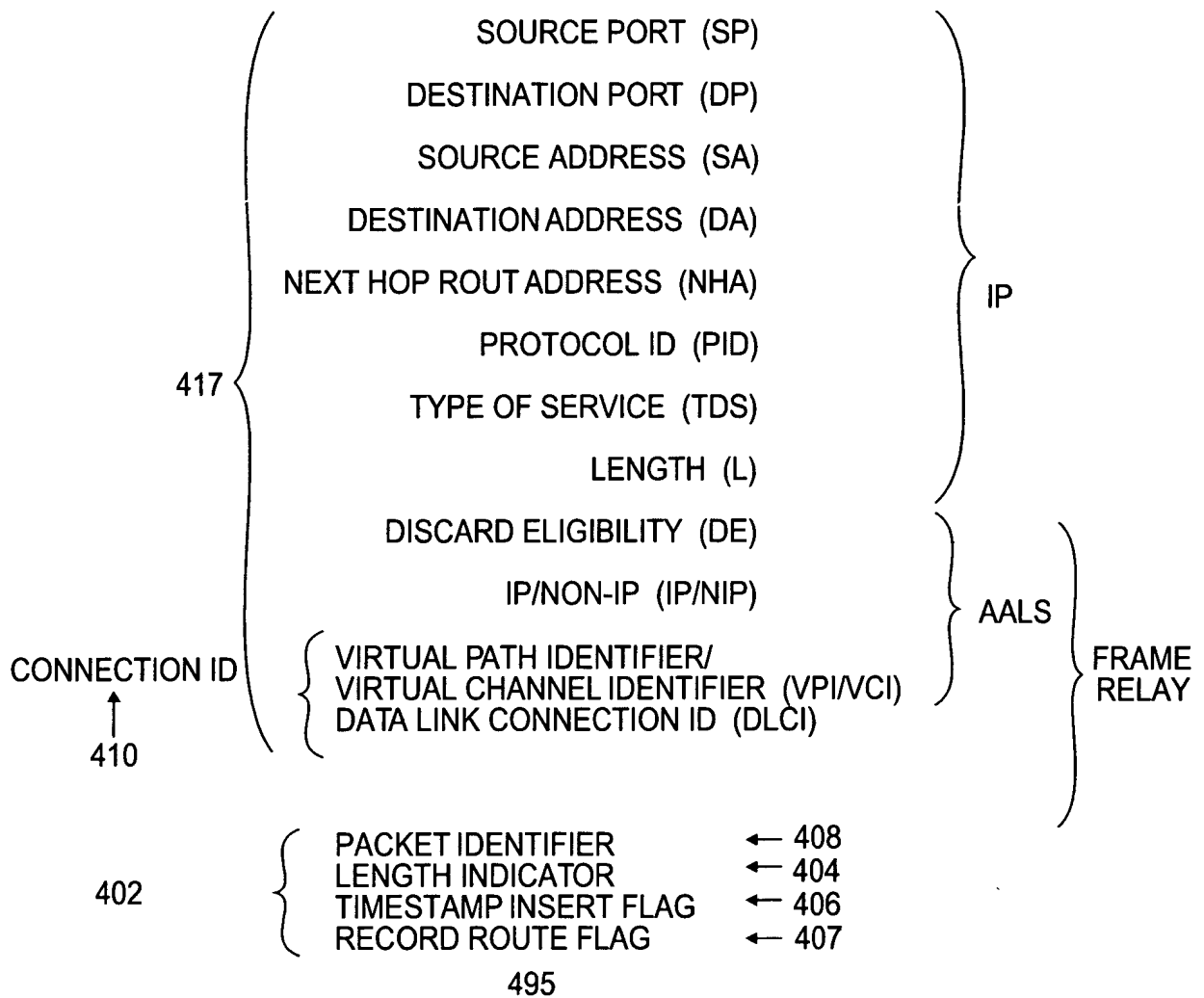


Fig. 4

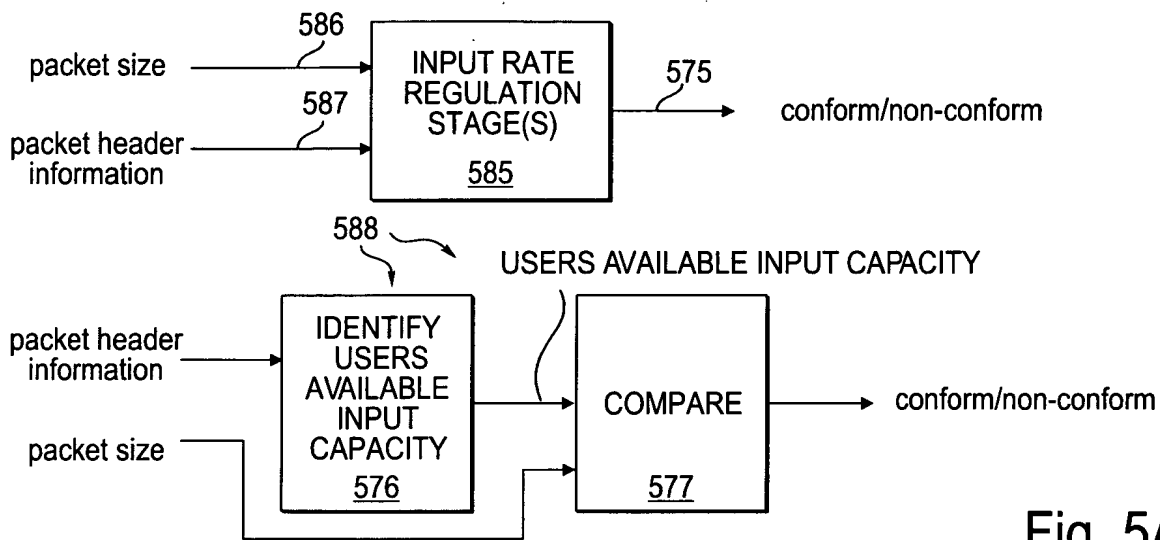


Fig. 5A

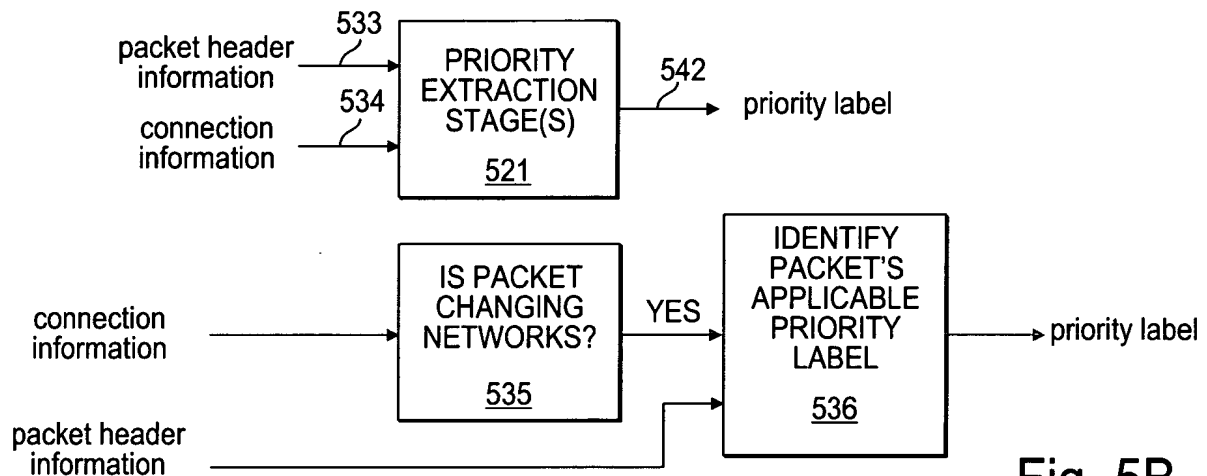


Fig. 5B

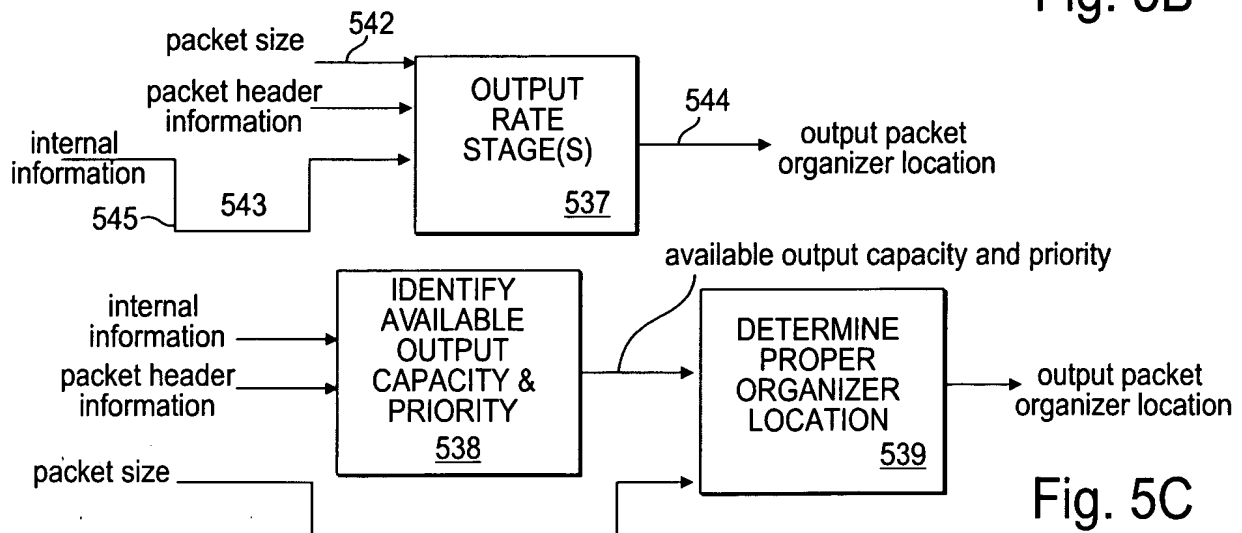


Fig. 5C

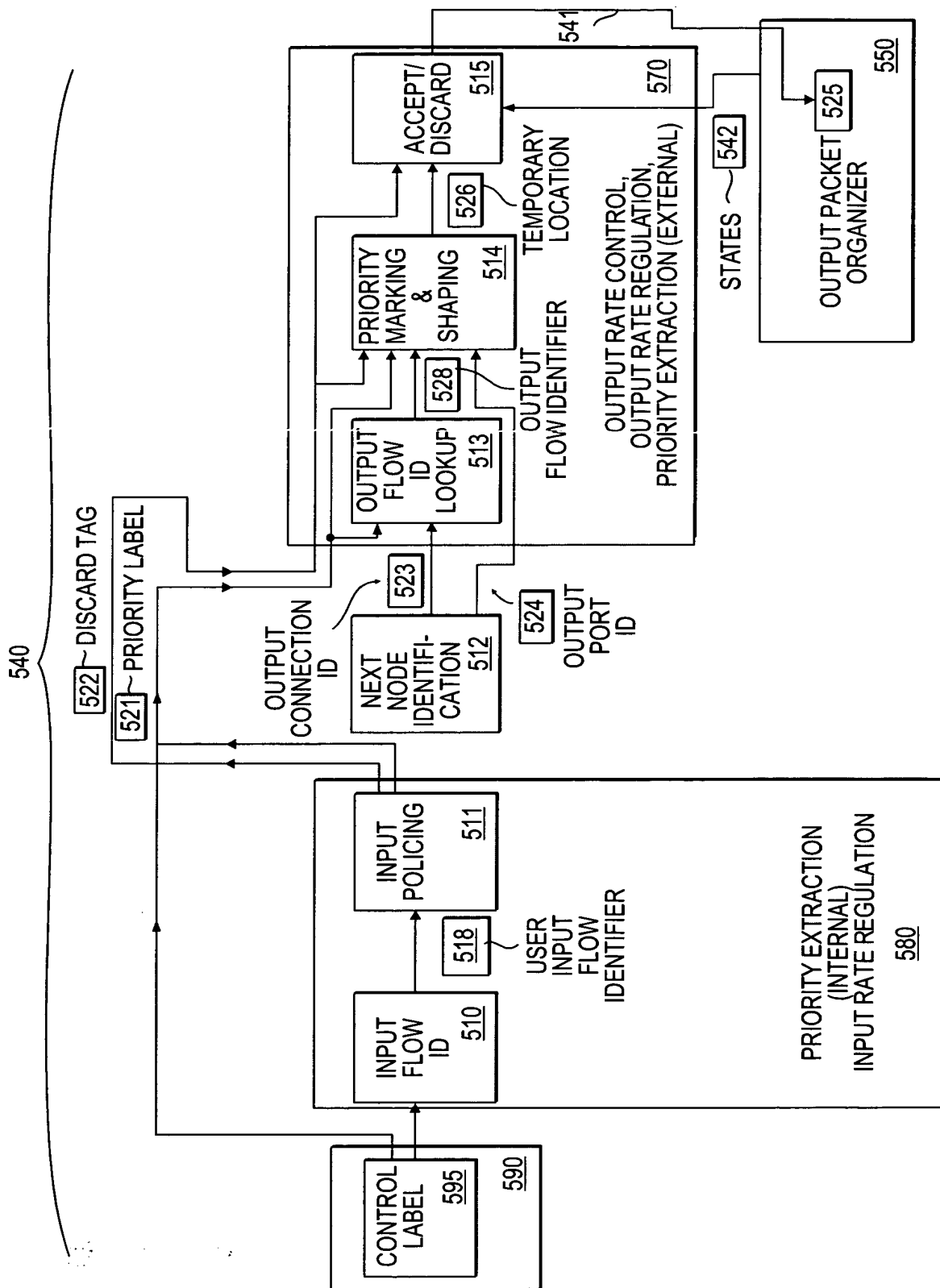


Fig. 5D



INPUT FLOW ID STAGE	INPUT POLICING STAGE	NEXT NODE IDENTIFICATION STATE	OUTPUT FLOW ID STATE	PRIORITY MARKING AND SHAPING STAGE	ACCEPT/DISCARD STAGE
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Fig. 6A

X	X	X		X	X
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Fig. 6B

		X	X	X	X
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Fig. 6C

X	X	X	X	X	X
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Fig. 6D

		X		X	X
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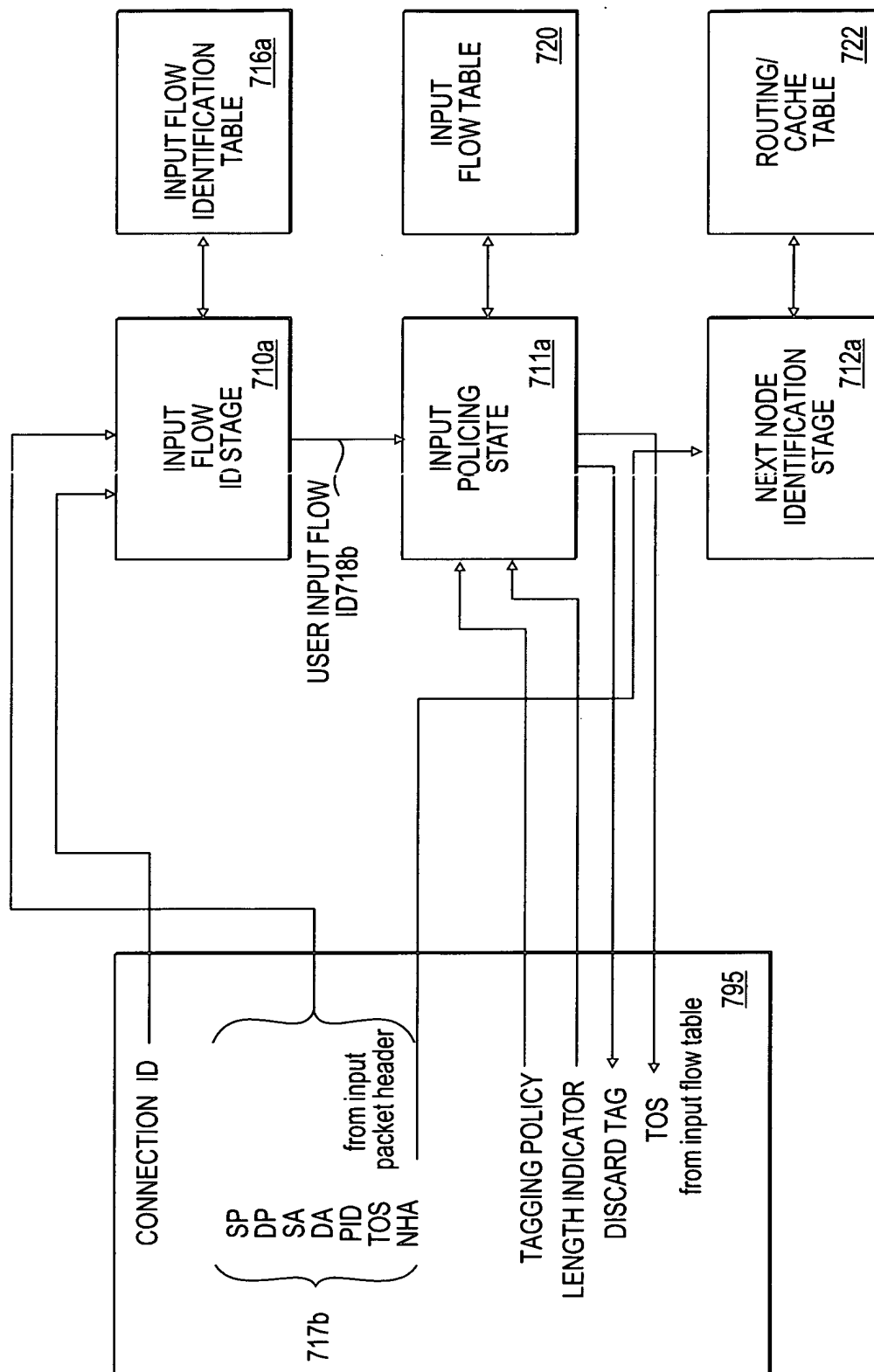
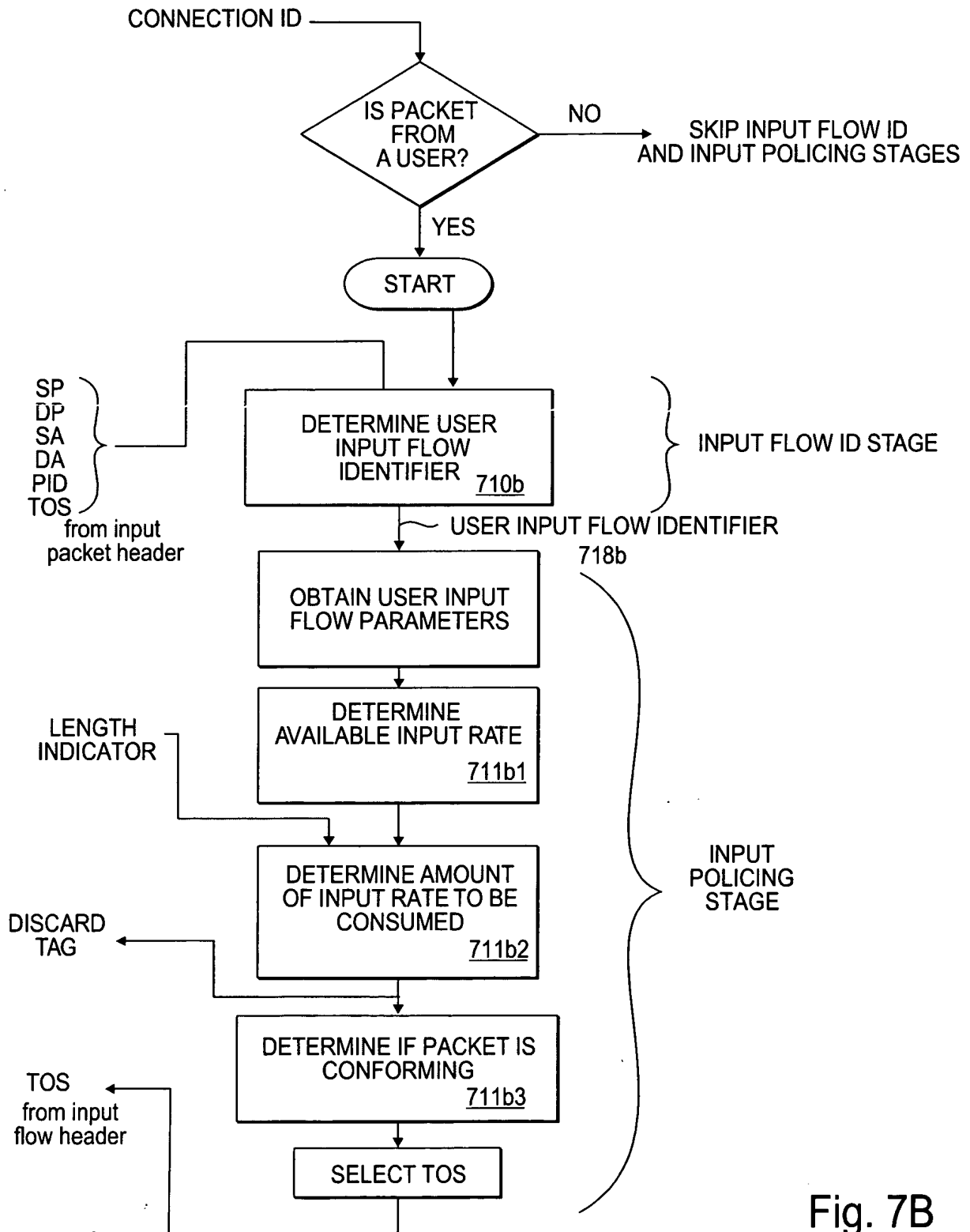


Fig. 7A



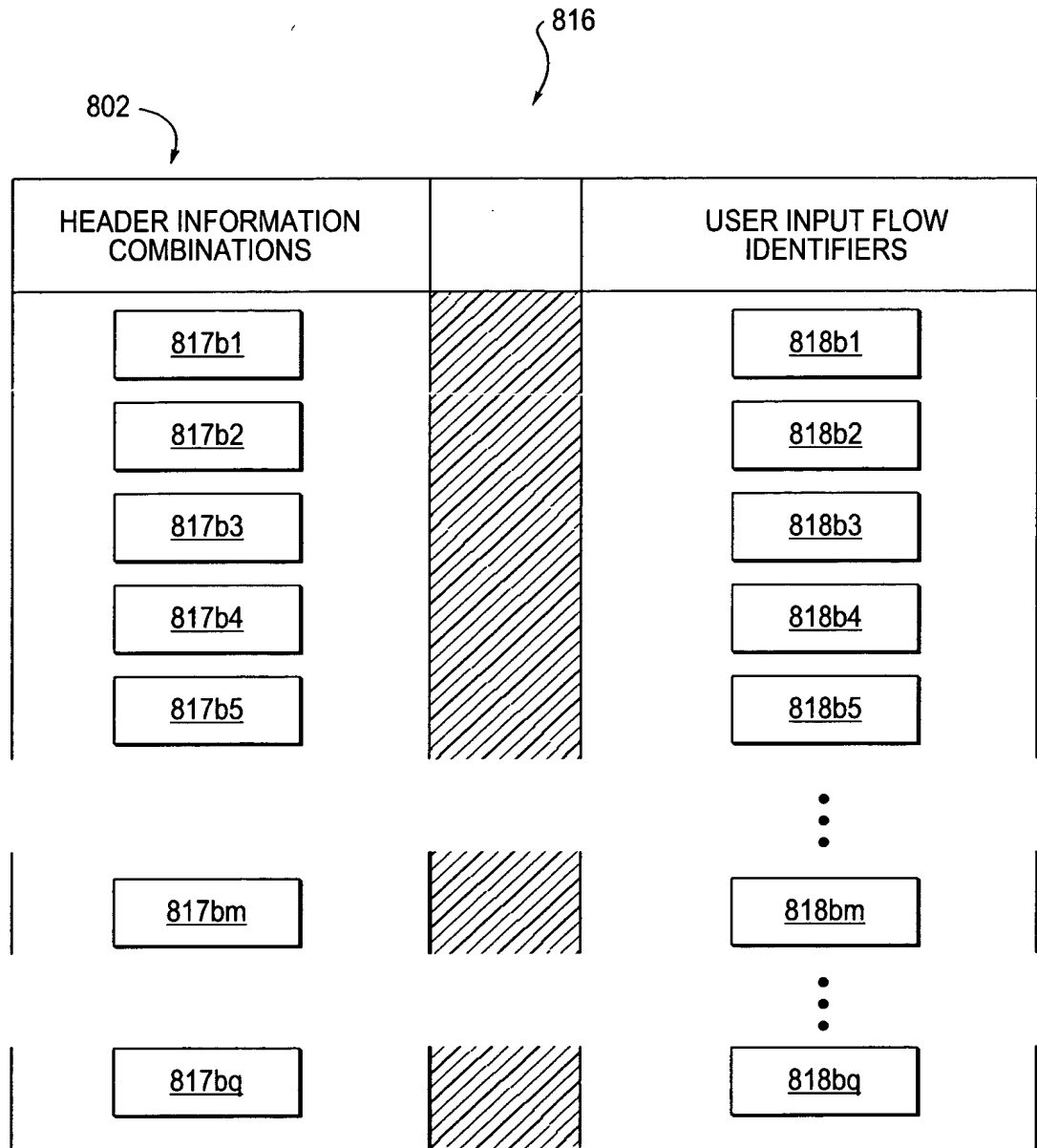


Fig. 8

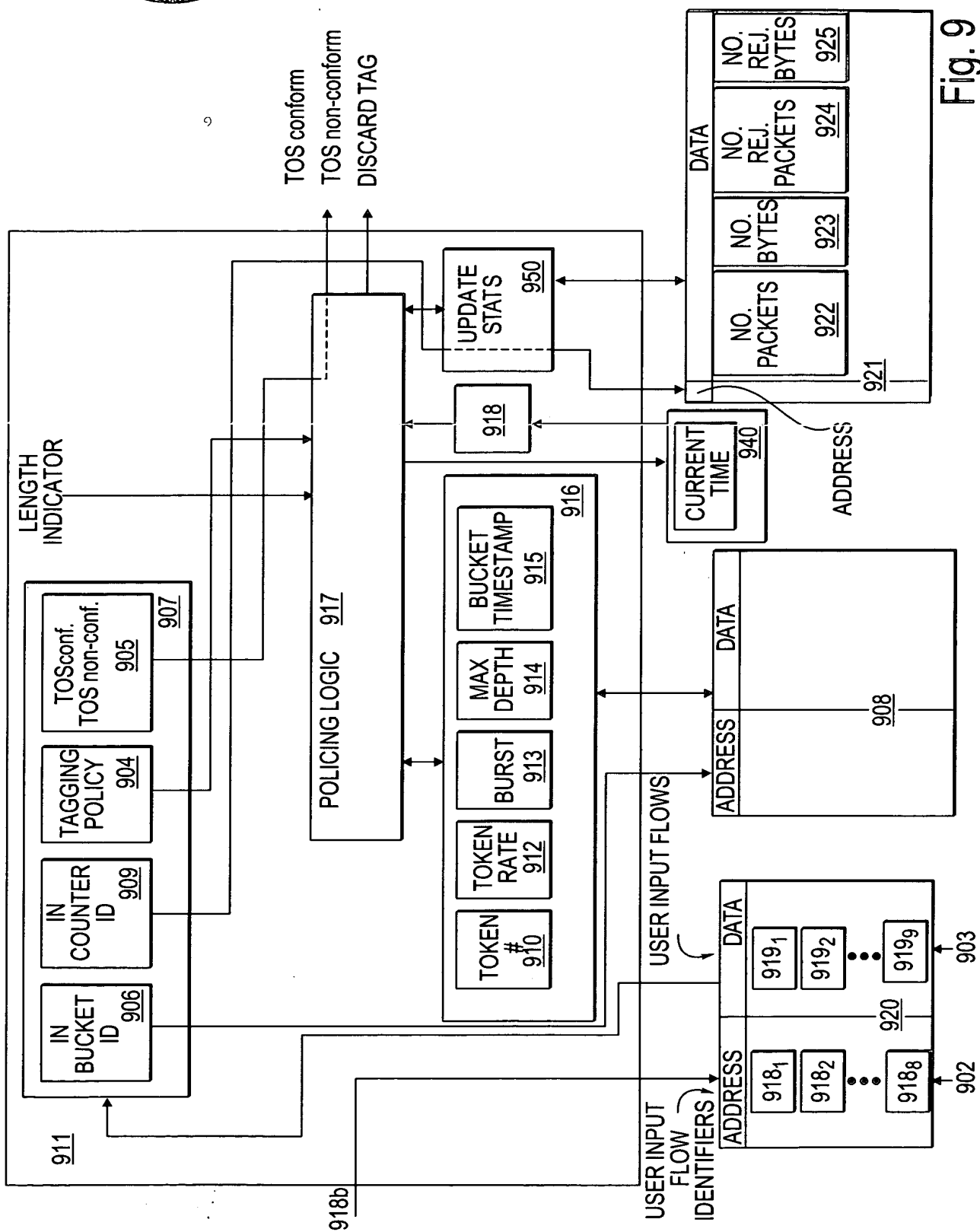


Fig. 9

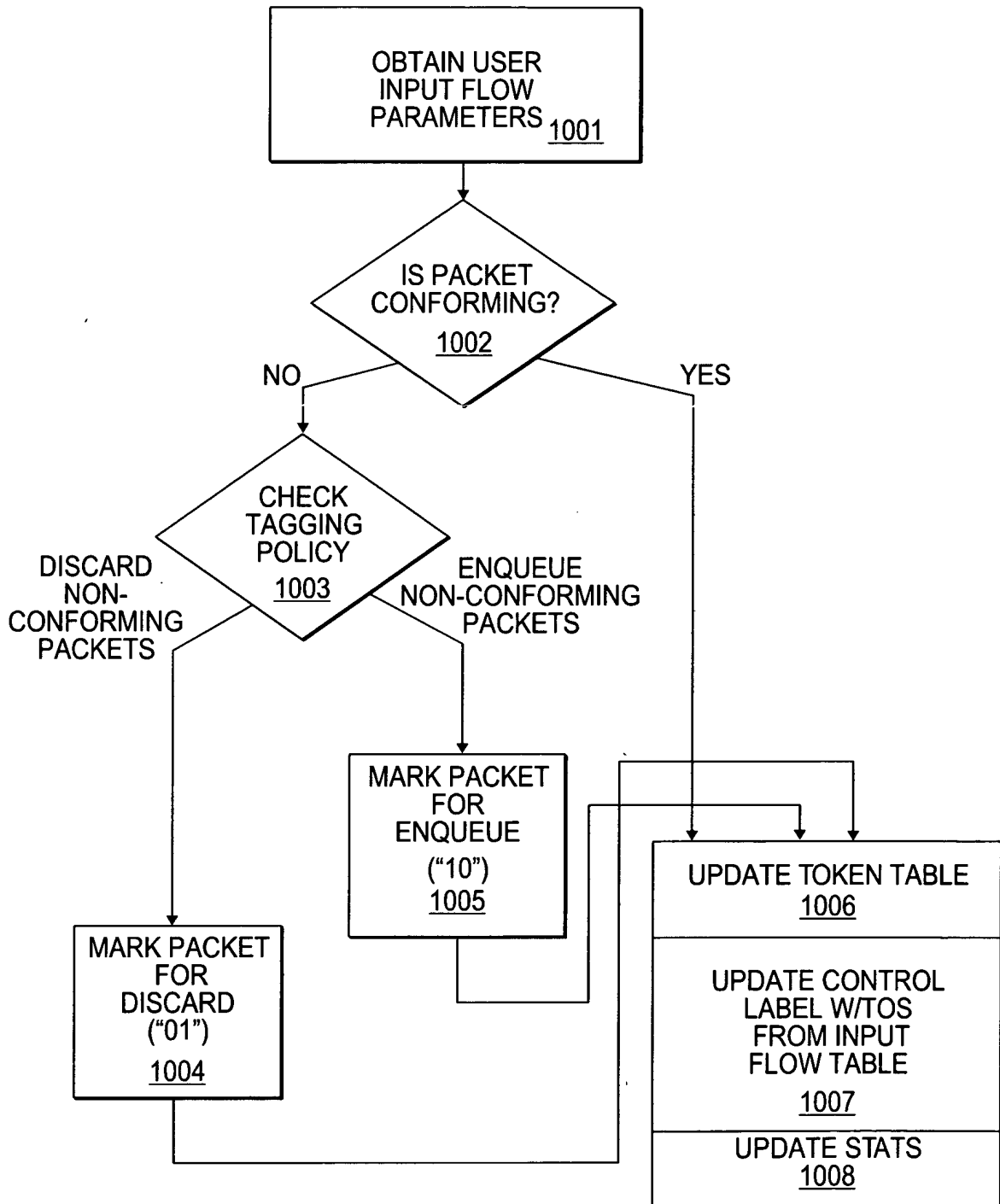
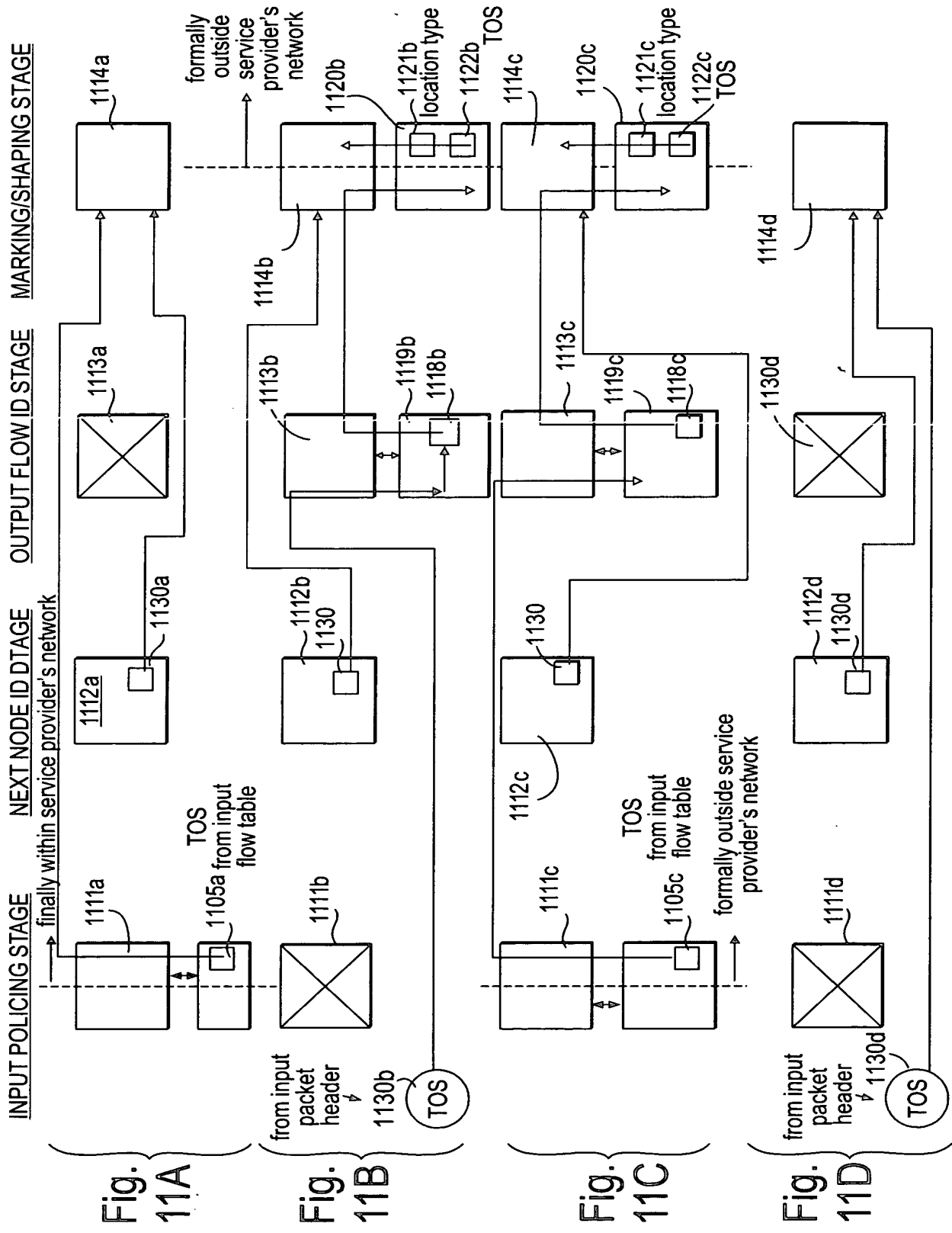
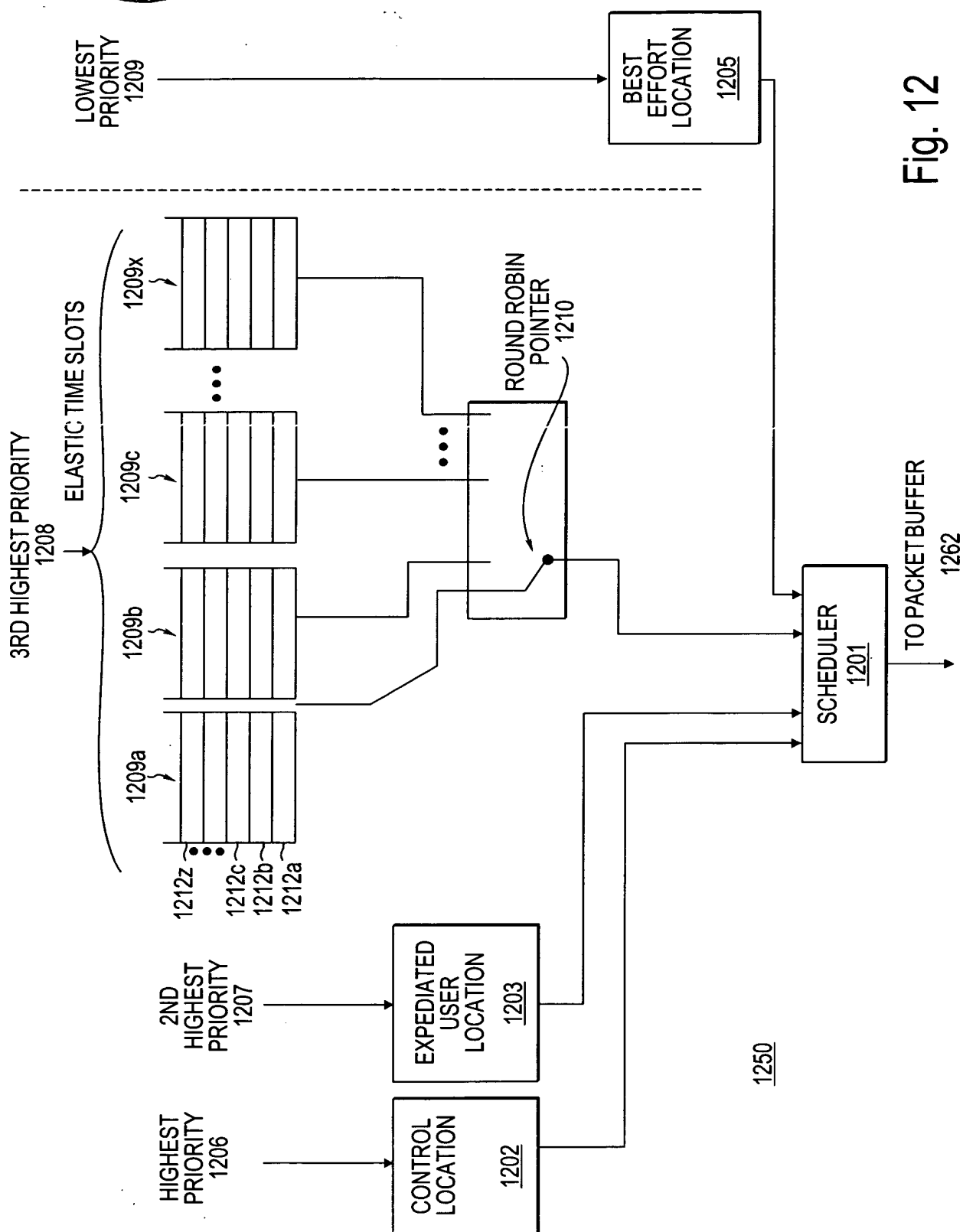


Fig.10





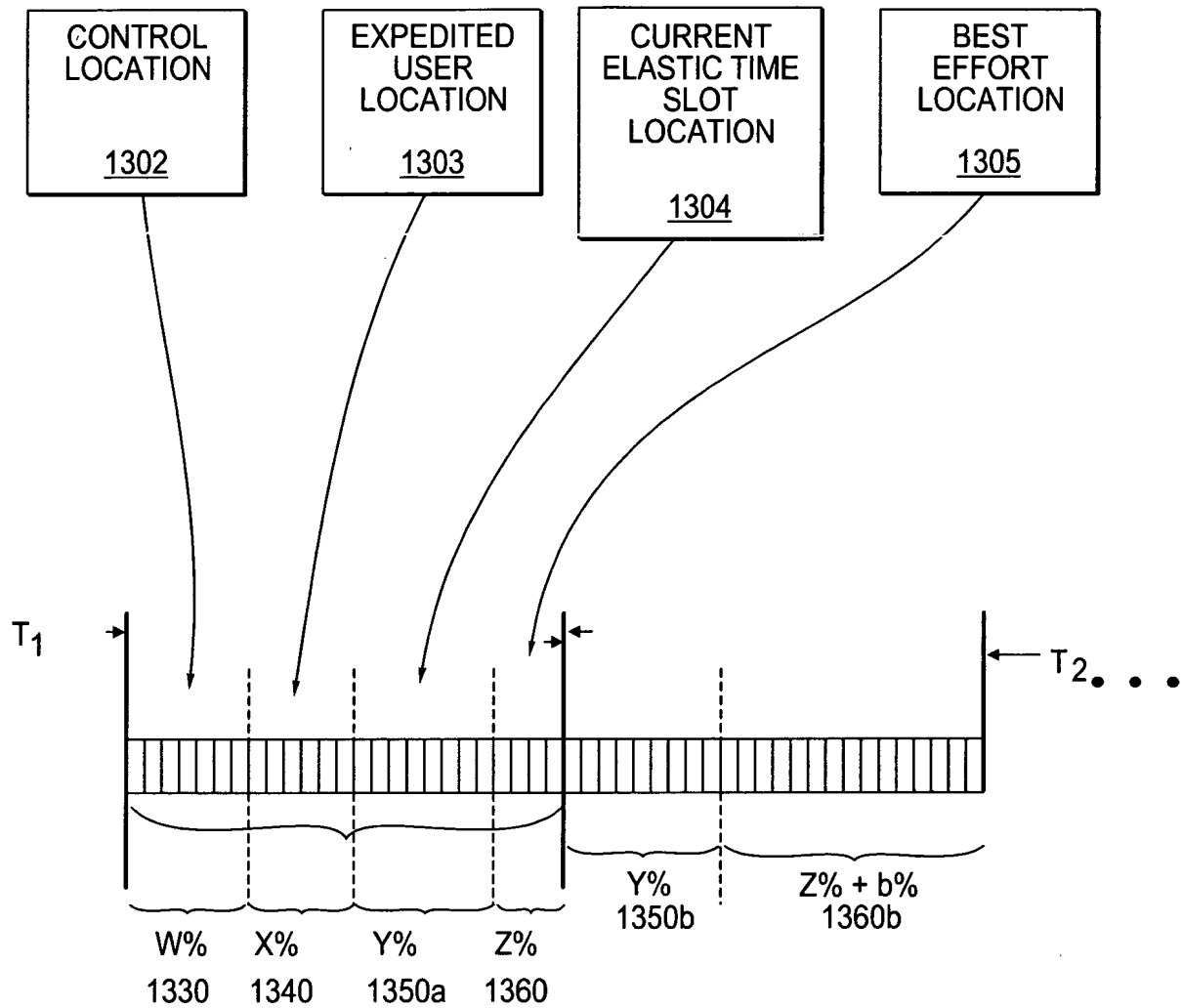


Fig. 13

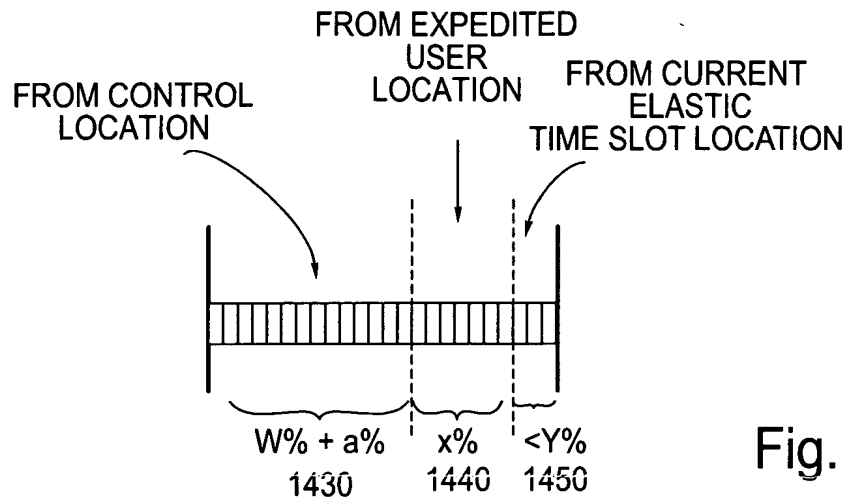


Fig. 14A

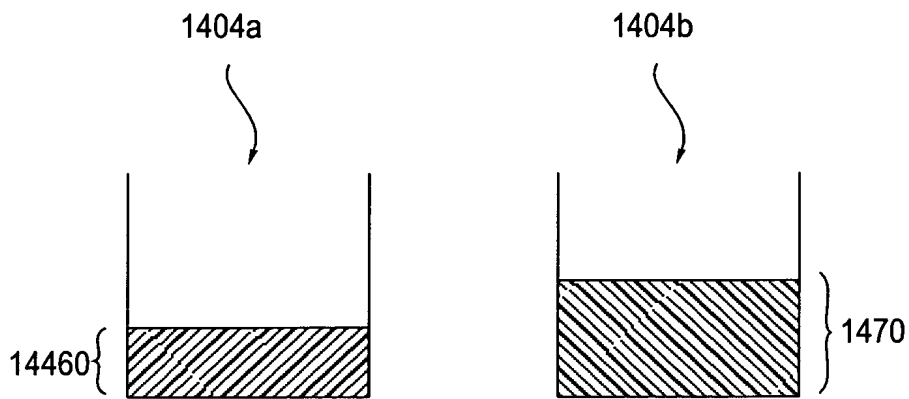


Fig. 14B

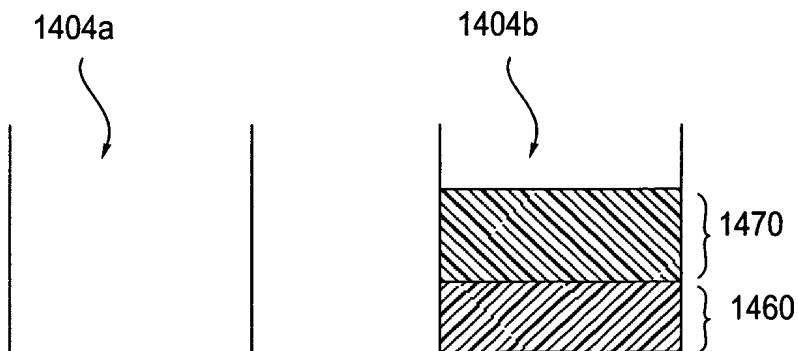


Fig. 14C

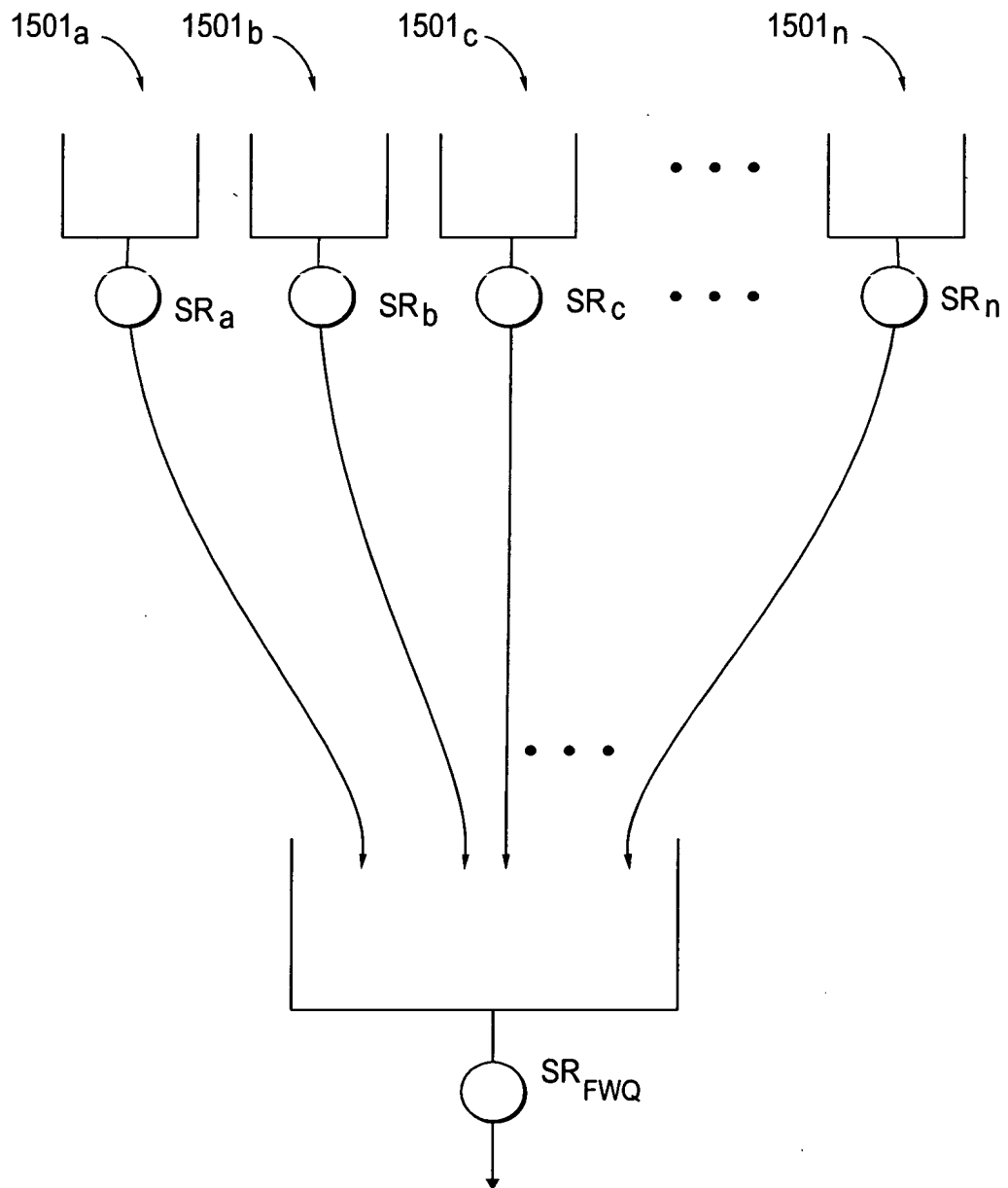


Fig. 15

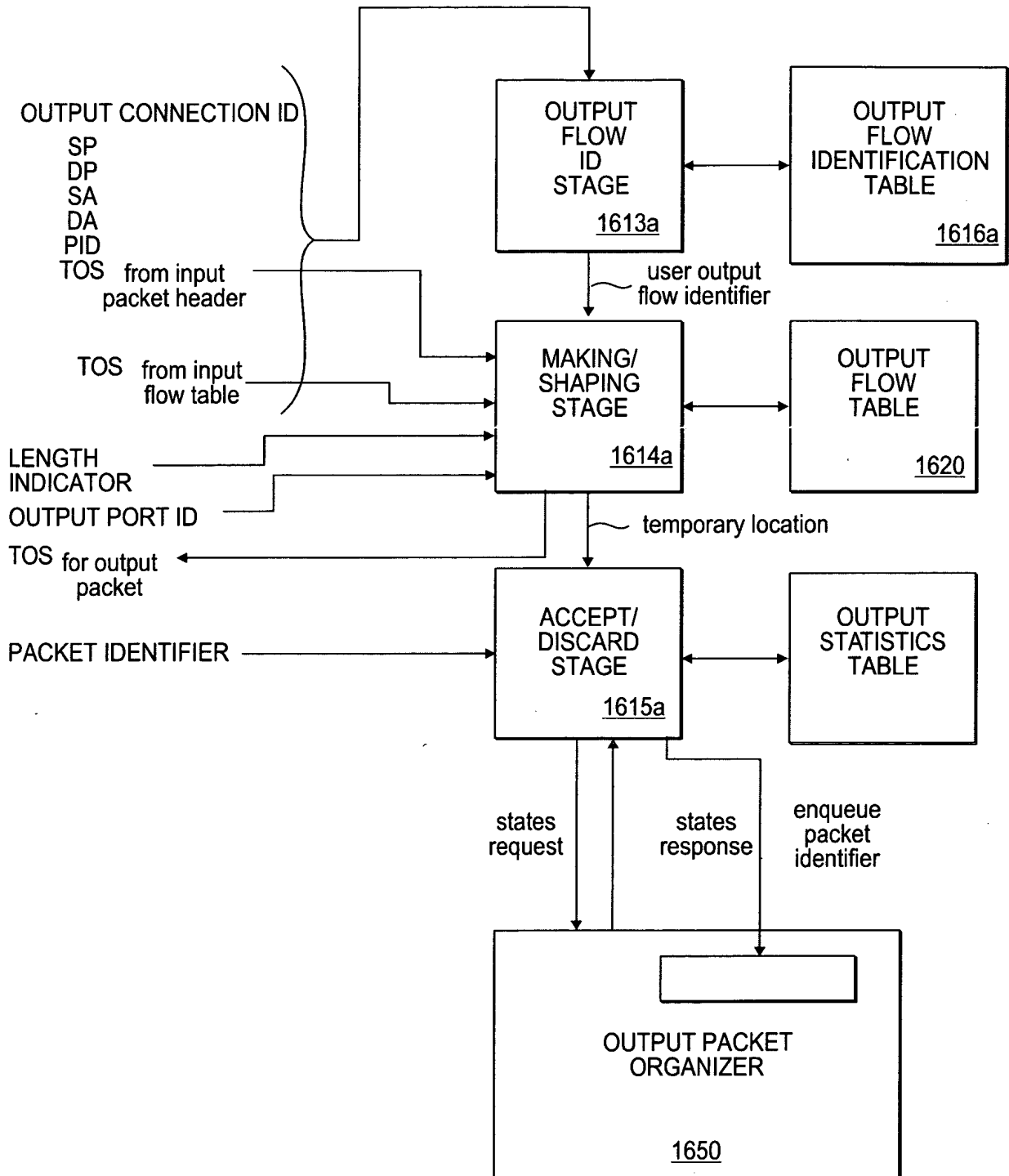


Fig. 16A

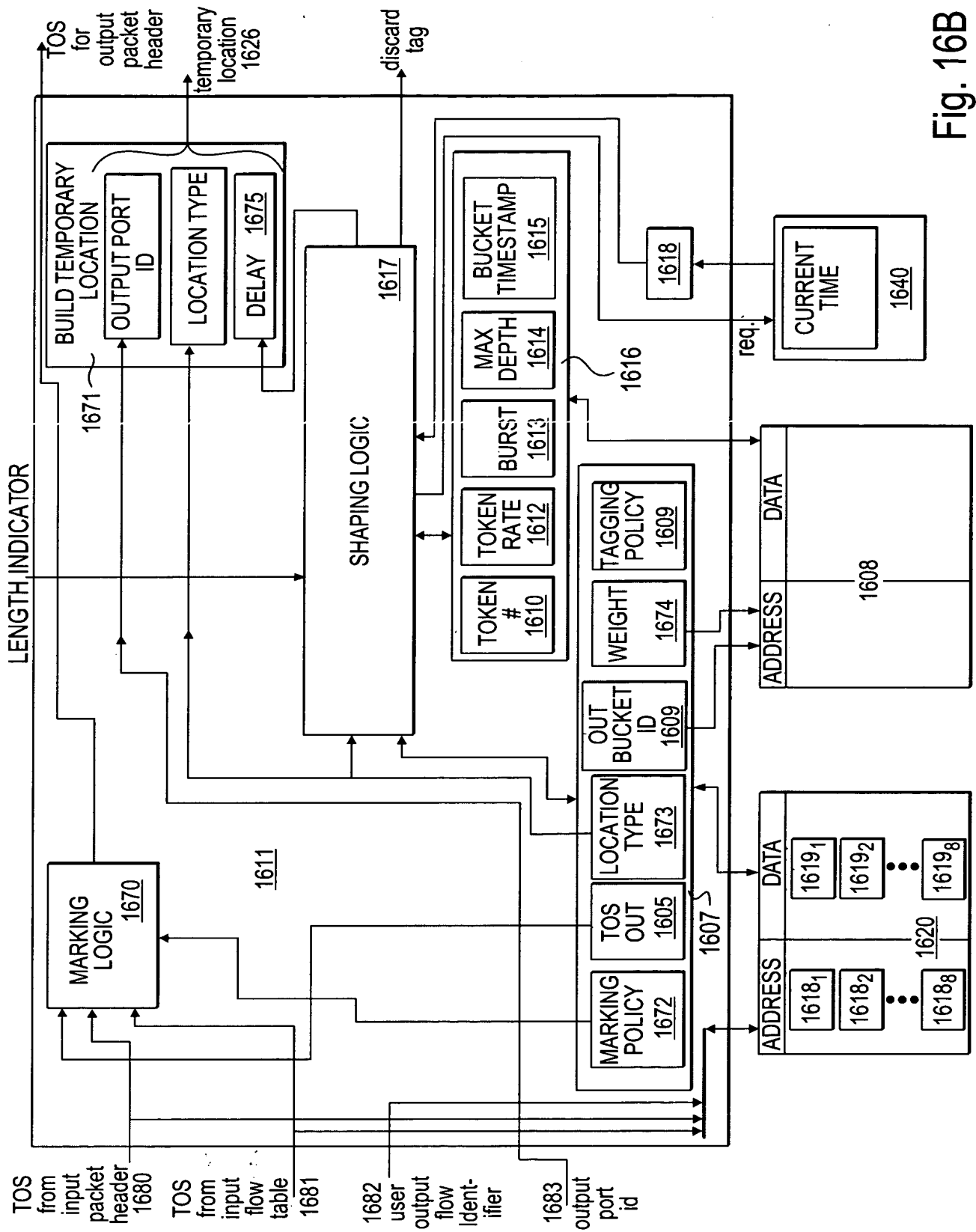


Fig. 16B

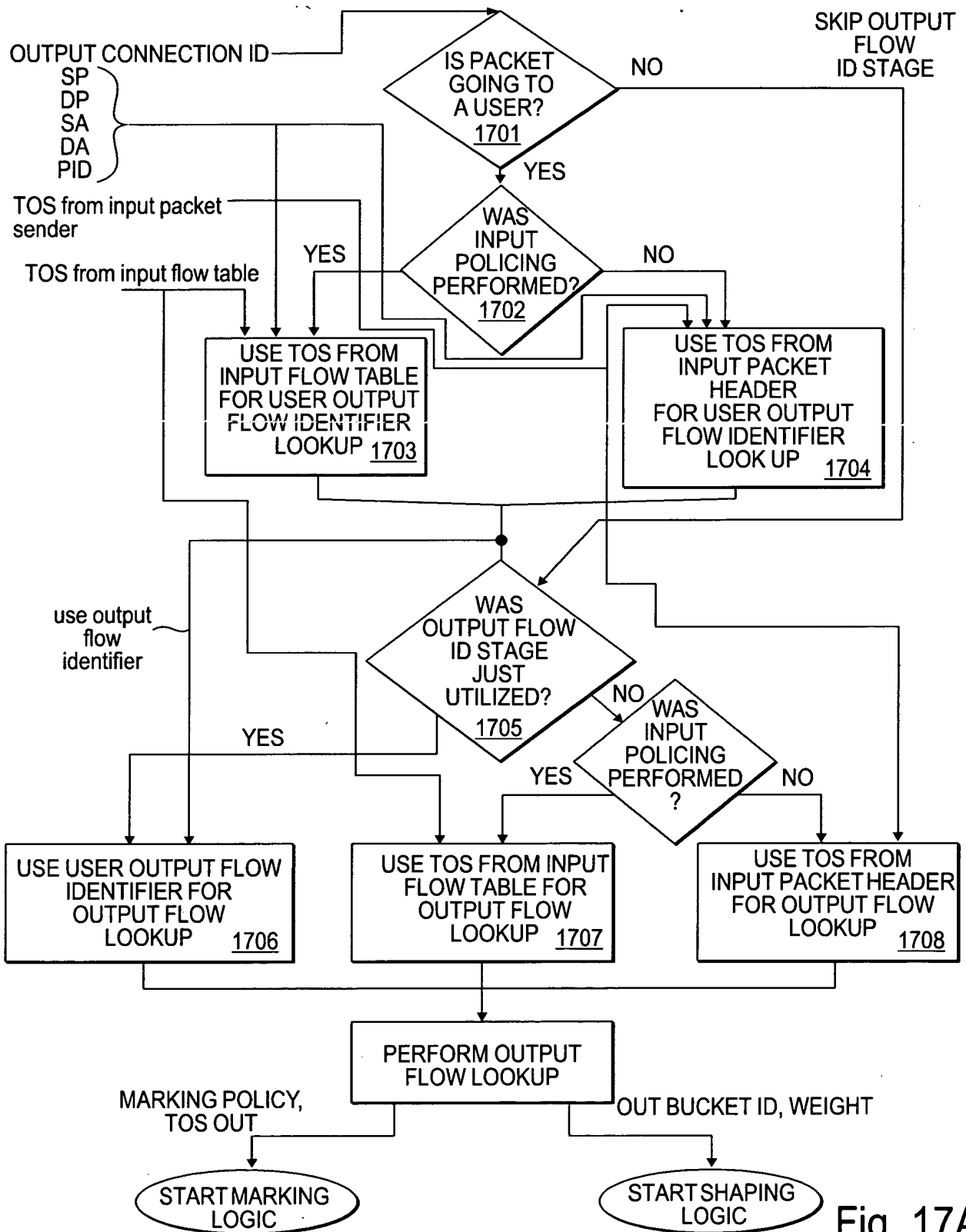


Fig. 17A

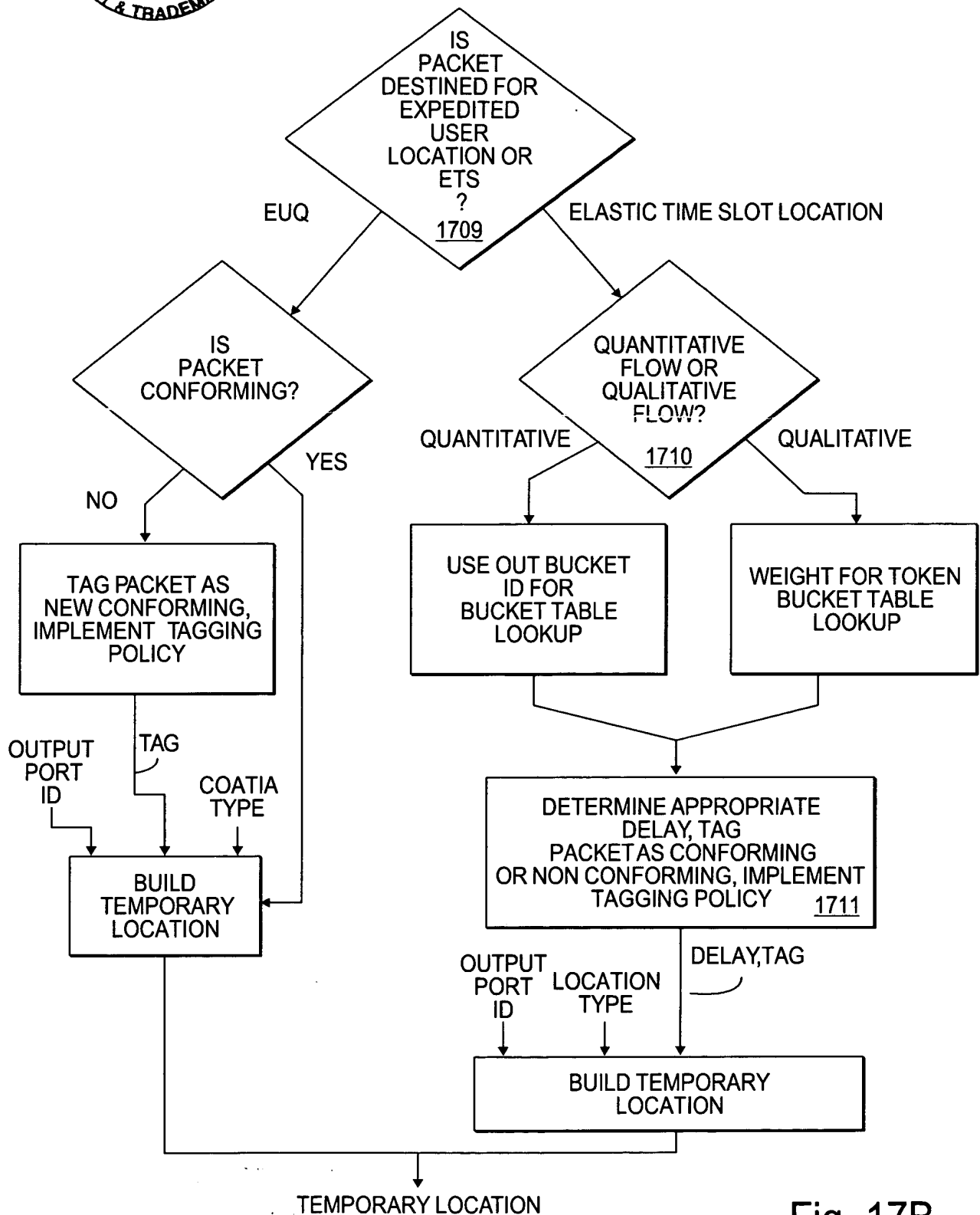


Fig. 17B



MARKING LOGIC

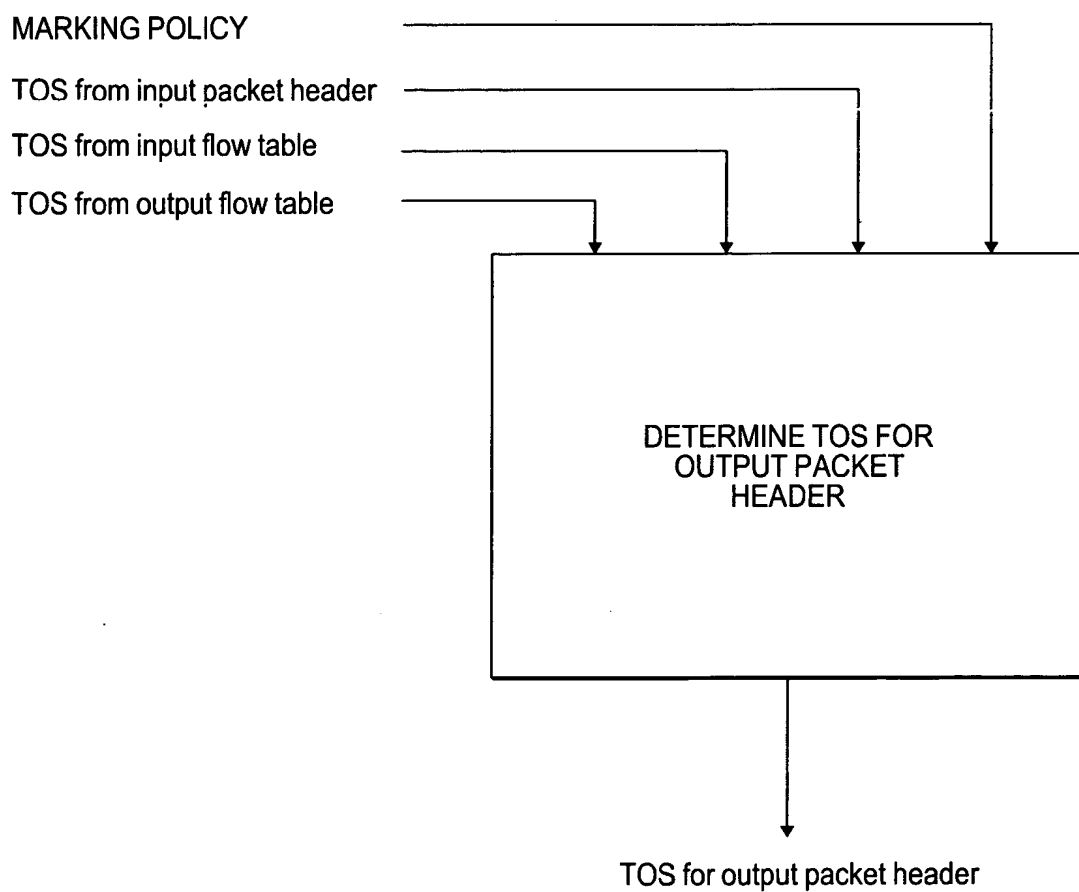


Fig. 17C

1800



ELASTIC TIME SLOT

EXPEDITED
USER
QUEUE

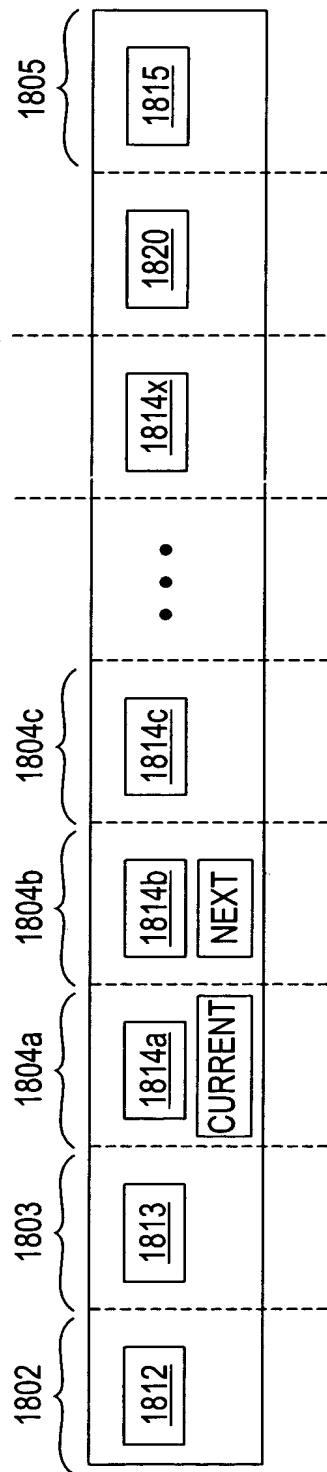


Fig. 18